Binary Coded Hexadecimal for a 7 Segment Display

EE 648: VLSI

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Introduction

The goal of this project is to design and fabricate a chip that will use 4 input bits to control a 7 segment display. The top level schematic for the project is shown in Figure 1.

[Top level schematic]

Note that each output (a-g) has it’s own set of logic gates. Many of the gate level circuits use the inputs as well as their complements. To reduce the number of gates in the final design, the inputs will each be inverted before being to the logic circuitry. This will minimize redundancies in the gate layout. This has not been included in this iteration of the design.

Truth Table and Logic Equations

The truth table for the four inputs and all seven outputs was created.

[Truth table goes here]

The truth table was transferred to the free software Logisim one output at a time. Logisim analyzed the truth table for each output bit and generated a minimized NAND Boolean expression. The expressions below have been modified to only include NAND, NOR and inverter gates.

[Boolean expressions go here]

Gate level schematic

These expressions were then used to generate gate level schematics. The generated gate level schematics included many different gate types. They were altered to only include NAND, NOR, and inverter gates. The expressions previously listed reflect these changes.

[logic schematics for each output go here]

After each circuit was altered, Logism was used to verify that the changes did not impact the functionality of the schematic. Trust us, we did it.